HX422D

Radiation Hardened Quad RS422 Differential Line Driver

Features

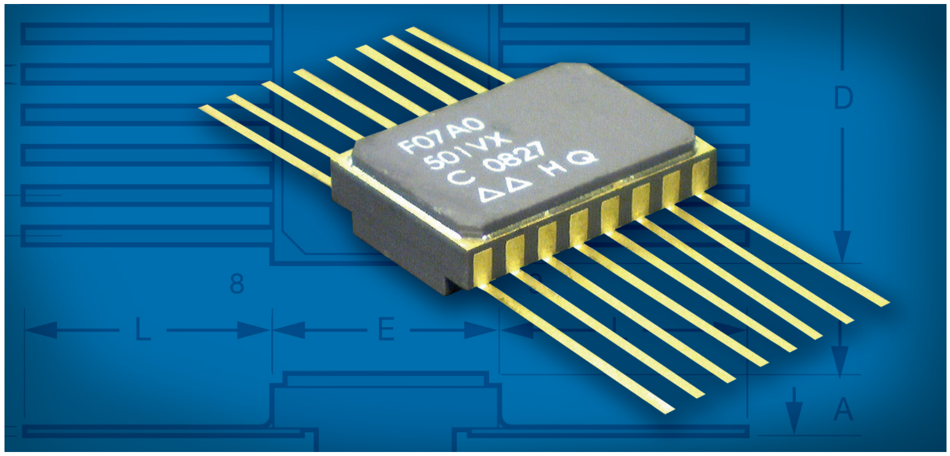
- Four Independent Drivers
- Rad Hard: 300k Rad(Si) Total Dose
- Single +3.3 V Power Supply
- Three-state Outputs
- Common Driver Enable Control
- Minimum Output Differential Voltage: 2V
- Temperature Range: -55°C to +125°C
- Maximum Operating Frequency: 20MHz
- Maximum Propagation Delay: 15ns
- 16 Lead Ceramic Flat Pack

Low Power

The HX422D dissipates less than 1mW in standby mode with no load.

Common Driver Enable Control (EN, EN*)

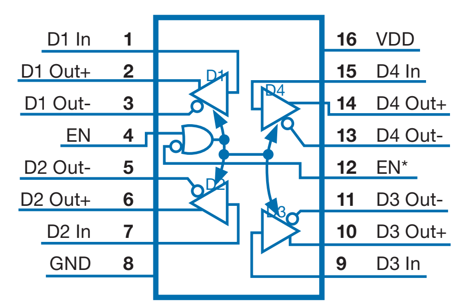
The EN and EN* inputs allow the user to put the digital outputs into a high impedance state.



The HX422D is a radiation hardened 3.3V CMOS quad differential line driver designed to meet the standard RS422 requirements and digital data transmission over balanced lines.

The HX422D is manufactured SOI-IV Silicon On Insulator (SOI) process with very low power consumption. It features four independent drivers with a common driver enable control and high impedance outputs. The EN and EN* inputs allow active low or active high control of the three-state outputs. The dual enable scheme allows for flexibility in turning devices on or off. The HX422D accepts 3V CMOS input levels and translates them into differential output voltage signals. The HX422D guarantees a minimum output differential voltage of 2V.

Package Pinout



Signal Definition

Signal	Definition
D1 In, D2 In D3 In, D4 In	Single ended CMOS digital data input pins
D1 Out+, D1 Out- D2 Out+, D2 Out- D3 Out+, D3 Out- D4 Out+, D4 Out-	Differential output pins
EN, EN*	Single ended CMOS digital input pins (output enable control pins) High Impedance: EN = L and EN* = H Normal Operation: All other combinations of EN and EN*

Truth Table

EN	EN*	Data	Q+	Q-
L	H	X	Z	Z
H	X	L	L	H
X	L	L	L	H
H	X	H	H	L
X	L	H	H	L

Absolute Maximum Ratings (1)(2)(6)

Parameter	Symbol	Conditions	Ratings Min	Ratings Max	Units
Maximum Continuous Current Per Output Pin			-70	70	mA
Supply Voltage	V_{DD}	—	-0.5	+6.5	V
DC Input Voltage	V_{IN}	—	-0.5	V_{DD} + 0.5	V
DC Output Voltage (3)	V_{OUT}	—	-0.5	V_{DD} + 0.5	V
Input Diode Clamp Current	I_{ik}	VI < 0-VTH_diode or			
		VI > VDD + VTH_diode	-180	+180	mA
Output Short Circuit Current (4) (5)	Ios	D1 Out+, D1 Out-, D2 Out+, D2 Out-			
		D3 Out+, D3 Out-, D4 Out+, D4 Out-			
		VOUT = 0.0 V, Enabled EN = H	30	300	mA
DC Output Current, Per Pin	I_{OUT}	VO= 0 to VDD		+70	mA
Thermal Resistance, Junction to Case	θ_{JC}	—	—	+22.2	°C/W
Storage Temperature Range	T_{STG}	—	-65	+150	°C
Lead Temperature Range (soldering, 4 seconds)	T_{LMAX}	—	—	+300	°C
Junction Temperature	T_J	—	—	+175	°C
ESD (Human Body Model)	—	—	—	2000	V

(1) Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
(2) Manufacturer does not guarantee the operation of the part in this manner. Temporary operation of input pins above or below the rails during a dose event could (though unlikely) compromise the total dose capability of the part.
(3) RS422 Transmit Buffer must withstand a disabled or un-powered RS422 Receiver for an unlimited period of time, without being damaged.
(4) Output Short Circuit not intended to imply continuous operation.
(5) Transmitter shall withstand without damage the application of short circuit across its output terminals, or from any output to circuit ground for at least 5 minutes. The transmitter should resume normal operation when the short is removed. One output at a time should be shorted and the maximum junction temperature should not be exceeded.
(6) All unused inputs of the device must be held at VDD or GND to ensure proper device operation.

Recommended Operating Conditions (1)(2)

Parameter	Symbol	Limit Min	Limit Max	Units
Supply Voltage	V_{DD}	3.0	3.6	V
Case Operating Temperature	T_C	-55	+125	°C
High Level Input Voltage	V_{IH}	0.7 x VDD	V_{DD}	V
Low Level Input Voltage	V_{IL}	0	0.3 x VDD	V
Input Voltage	V_{IN} CMOS	-0.3	VDD + 0.3	V
Output Voltage	V_{OUT}	-0.3	VDD + 0.3	V

(1) All unused inputs of the device must be held at VDD or GND to ensure proper device operation.
(2) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.

Radiation Hardness Ratings (1)

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose	TID		300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse width ≤ 20ns	$1x10^9$	rad(Si)/s
Dose Rate Survivability	DRS	Pulse width ≤ 20ns	$1 x10^{12}$	rad(Si)/s
Neutron Fluence		1MeV equivalent energy	$1 x10^{14}$	N/cm^2

(1) Device will not latch up due to any of the specified radiation exposure conditions.

Radiation Characteristics

Total Ionizing Dose Radiation
The device radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation
Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage
SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup
The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Electrical Requirements

Parameter	Symbol	Conditions		Limit Min	Limit Max	Units
Output Differential Voltage	V_{D1}	No Load		—	3.6	V
Output Differential Voltage	V_{D2}	R_L = 100 Ω		2.0	—	V
Output Differential Voltage Change	ΔV_{D2}	I_{OUT} 0 – 20 mA		-0.4	0.4	V
Common Mode Voltage	V_{CM}	R_L = 100 Ω		—	2	V
Common Mode Voltage Change	ΔV_{CM}	R_L = 100 Ω		-0.4	+0.4	V
Three-state Output Leakage High	I_{OZH}	$V_{OUT} = V_{DD}$, disabled		—	20	µA
Three-state Output Leakage Low	I_{OZL}	V_{OUT} = 0.0 V, disabled		-20	—	µA
Output High Voltage	V_{OH}	I_{OUT} = -20 mA		2.0	—	V
Output Low Voltage	V_{OL}	I_{OUT} = 20 mA		—	0.5	V
Input Threshold High	V_{IH}	V_{DD} = 3.6 V, ($V_{IHMIN} = 0.7*V_{DD}$)		2.5	—	V
Input Threshold Low	V_{IL}	V_{DD} = 3.0 V, ($V_{IHMAX} = 0.3*V_{DD}$)		—	0.9	V
Input Leakage Current High	I_{IH}	V_{DD} = 3.6V, Vin = 3.6V		-10	10	µA
Input Leakage Current Low	I_{IL}	V_{DD} = 3.6V, Vin = 0V		-10	10	µA
Input Clamp Diode Voltage	V_{IKL}	I_{IN} = -20 mA, V_{DD} = 0V		-1.5	—	V
	V_{IKH}	I_{IN} = 20 mA, V_{DD} = 0V		—	+1.5V	V
Standby Current	I_{DDSB}	V_{DD} = 3.6V, No Load, Inputs = 0 V or V_{DD}		—	150	µA
Operational Supply Current	IDDOP1	VDD = 3.6V, CL = 85pF	1MHz		140	mA
	IDDOP10	RL = 100 ohms	10MHz		230	mA
	IDDOP20	All outputs toggling	20MHz		280	mA

Capacitance Parameters (1)

Symbol	Parameter	Limits Min	Limits Max	Units
C_I	Input Capacitance CMOS Inputs		12	pF
C_O	Output Capacitance (pin to ground)		20	pF

(1) Capacitance is guaranteed by design.

Switching Requirements

Symbol	Parameter	Limit Min	Limit Max	Units
t_{pwd} (1)(2)(3)	Driver output jitter		650	ps
t_{pwd_in} (1)(2)(3)	Driver output jitter with power supply noise		800	ps
t_{PHLD} (3)	Differential Propagation Delay High to Low	0.25	15	ns
t_{PLHD} (3)	Differential Propagation Delay Low to High	0.25	15	ns
t_{SKD} (1)	Differential Pulse Skew (same channel) $\|t_{PHLD} - t_{PLHD}\|$		3	ns
ΔSK_{CC1} (1)	Differential Channel-to-Channel Skew		3	ns
t_{TLH} (1)(3)	Differential Output Transition Time Low to High (20% to 80%)		10	ns
t_{THL} (1)(3)	Differential Output Transition Time High to Low (20% to 80%)		10	ns
t_{PHZ} (4)	Disable Time High to Z		20	ns
t_{PLZ} (4)	Disable Time Low to Z		20	ns
t_{PZH} (4)	Enable Time Z to High	0.25	20	ns
t_{PZL} (4)	Enable Time Z to Low	0.25	20	ns
F_{max}	Max Operating Frequency		20	MHz

(1) Guaranteed but not tested in production.
(2) Maximum RS422 Driver Jitter performance is guaranteed between -5°C and 125°C case temperature, between 3.0 V and 3.6 V; and pre- and post-radiation.
(a) Driver CMOS input signal transition time of 1.0 ns, 10%-to-90% for a 0 V - V_{DD} waveform.
(b) Apply a minimum of 250 Pseudo Random Bit Stream (PRBS) bits, at 25 Mbps rate, with no more than 10 consecutive non-transitioning bits in the data stream, at RS422 driver CMOS input. Refer to diagrams below.
(c) Measure peak-to-peak data jitter at RS422 driver output across the 100 Ω resistor.
(d) All jitter measurements will be made with a sample size of 100,000 and a Bit Error Rate of 1E-12.
(3) Refer to Figure 1. (RL=100 Ohms, CL=50pF).
(4) Refer to Figure 2. (CL=50pF).

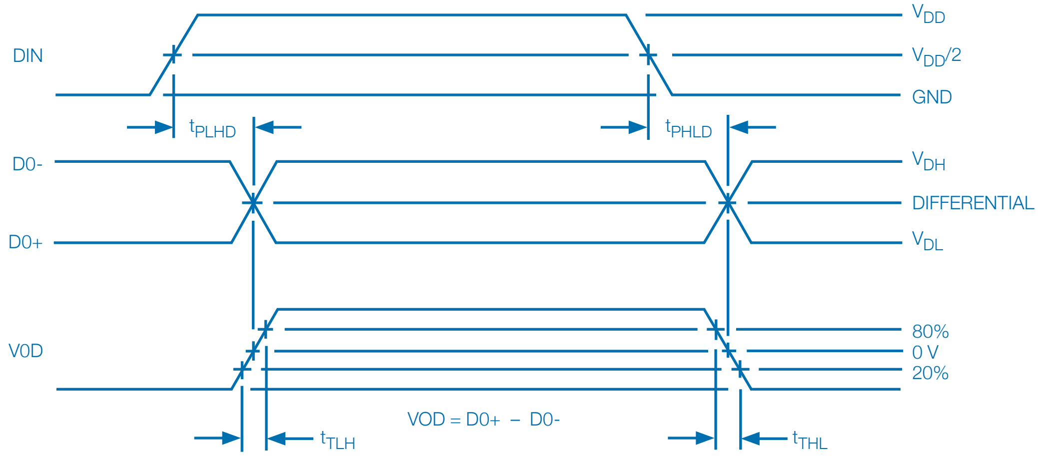
Signal Integrity

As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

Timing Diagrams

Differential Driver Propagation Delay, Jitter and Transition Time



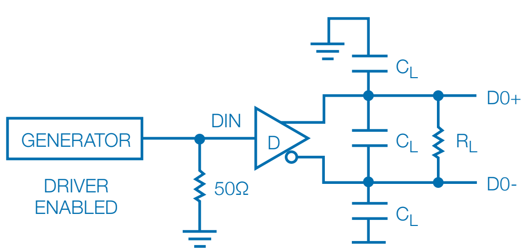


Figure 1

Note: Reference load only, not used for production test.

Differential Driver Single-Ended Three-State

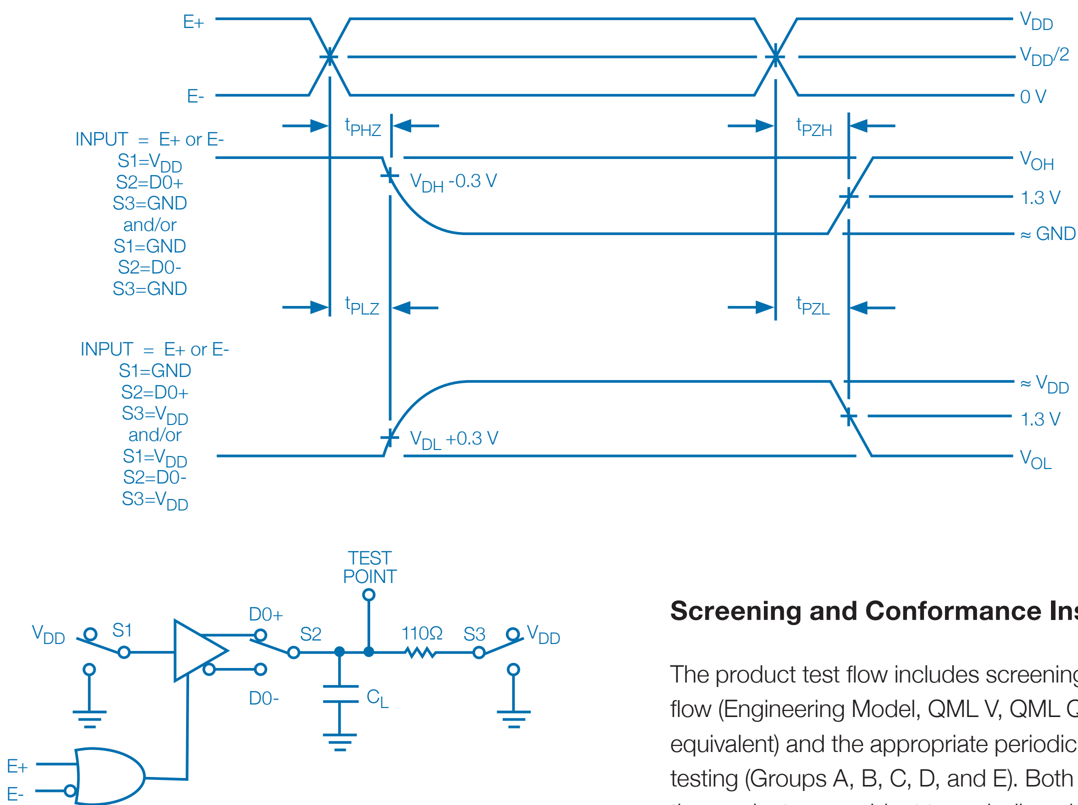


Figure 2

Note: Reference load only, not used for production test.

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

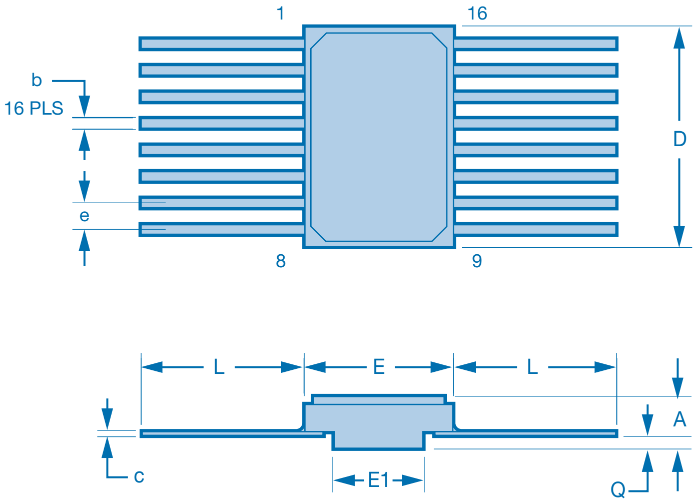
Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Conformance Summary

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Package Outline Dimensions



Symbol	Dimensions - Inches Min	Dimensions - Inches Max	Dimensions - Millimeters Min	Dimensions - Millimeters Max
A	.101	.125	2.57	3.18
b	.015	.019	0.38	0.48
c	.004	.007	0.11	0.18
D	.392	.408	9.96	10.36
e	.047	.053	1.20	1.34
E	.274	.286	6.96	7.26
E1	.185	.196	4.70	4.96
L	.320	.360	8.13	9.14
Q	.022	.032	0.56	0.82

Ordering Information

Standard Microcircuit Drawing

The HX422D can be ordered under the SMD drawing 5962-07A05.

H X 422 D G V F

Source
H = Honeywell

Process
X = SOI CMOS

Part Number

Part Type
D = Driver

Package Designation
G = 16 Pin Flat Pack

Screen Level
V = QML V
W = QML Q+
E = Eng. Model (2)

Total Dose Hardness
F = 3x10^5 rad (Si)
N = No Level Guaranteed (2)

(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywellmicroelectronics.com/

Honeywell Aerospace
Honeywell
12001 Highway 55
Plymouth, MN 55441
Tel: 1.800.323.8295
www.honeywellmicroelectronics.com/

ADS-14201 Rev. A
June 2014

Honeywell